EPITAXIAL GROWTH FOR WAVEGUIDE TAPERING

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present invention is related to commonly-assigned and co-filed U.S. Patent Application No. [Attorney Docket No. 42P13840] entitled "Method For Producing Vertical Tapers In Optical Waveguides By Over Polishing" by M. Salib, and to U.S. Patent Application No. [Attorney Docket No. 42P13842] entitled "Fabrication Of A Waveguide Taper Through Ion Implantation" by M. Salib *et al.*

FIELD OF THE INVENTION

[0002] The field of invention relates to optical communication devices in general; and, more specifically but not limited to waveguide tapers in optical devices.

BACKGROUND

[0003] Some optical devices may include a waveguide that is intended to be coupled to another waveguide or fiber having a significantly larger cross-sectional size. For example, a planar lightwave circuit (PLC) can have a waveguide on the order of four microns in width to be coupled an optical fiber with a diameter of about ten microns. One way to couple a port of a relatively large waveguide to a port of a significantly smaller waveguide is by forming a tapered waveguide structure to couple the two waveguides. In one type of taper, the taper at one end has a width or diameter of about the same size as the larger waveguide. At the other end, the

taper comes to a point. The sides of the taper are typically straight so that the taper has a wedge-like shape, with the taper narrowing from the wide end to the point or narrow end. The wide end of the taper is used to couple the taper from the larger waveguide. The idea behind this taper is to create a virtual, vertical effective index change in the waveguide that forces the mode into an underlying, single-mode waveguide. As the taper becomes narrower, the effective index decreases, and the mode moves lower in the semiconductor material.

[0004] One conventional technique to form the above-described taper when the smaller waveguide is a semiconductor waveguide is to etch one end of the smaller waveguide to form the taper. For example, at the end of the waveguide, the smaller waveguide has: (a) a length about equal to the desired length of the taper; and (b) a thickness that is about equal to the sum of the desired thickness of the smaller waveguide and the desired thickness of the taper. For example, the resulting thickness can be about the height of the core of an optical fiber. This end of the smaller waveguide is then etched using standard etching techniques to form the taper with a shape as described above. However, some etching processes form the taper's point so that it appears eroded, instead of the desired sharp edge or point. This erosion can degrade performance of the taper. In addition, typical etching processes cause the etched surfaces to be significantly less smooth than the surfaces that are not etched. This roughness can increase the waveguide's loss (e.g., in some tests the etched surfaces increased loss an addition five to ten decibels).

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following figures, wherein like reference numerals refer to like parts or elements having the same or substantially similar functions and/or structures throughout the various views unless otherwise specified. Further, terms such as "top", "upper", "lower", "vertical", "lateral", "beneath", etc. may be used herein in describing the figures. These terms are used in a relative sense to show relative orientation of the parts or elements as depicted in the figures and not necessarily with respect gravity or as physical embodiments may be oriented during use.

[0006] Figures 1 and 1A are representative cross-sectional and top views of an initial stage in fabricating a taper, according to one embodiment of the present invention.

[0007] Figures 2 and 2A are representative cross-sectional and top views of another stage in fabricating a taper, respectively, according to one embodiment of the present invention.

[0008] Figures 3 and 3A are representative cross-sectional and top views of still another stage in fabricating a taper, respectively, according to one embodiment of the present invention.

[0009] Figures 4 and 4A are representative cross-sectional and top views of yet another stage in fabricating a taper, respectively, according to one embodiment of the present invention.

[0010] Figure 5 is a representative isometric perspective view of a section cut as indicated in Figure 4, according to an embodiment of the present invention.

[0011] Figure 6 is a block diagram illustrating an exemplary system using a taper fabricating according to embodiments of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0012] Figure 1 illustrates a partial cross-section of a semiconductor workpiece (not to scale) during an early stage in fabricating a taper, according to one embodiment of the present invention. The workpiece includes a semiconductor substrate 10, an insulator layer 12, a silicon layer 14, and a protective layer 16. Silicon layer 14 is formed so as to serve as a waveguide. In one embodiment, silicon layer 14 is formed so as to serve as a rib waveguide.

[0013] More particularly, insulating layer 12 is formed between semiconductor substrate 10 and silicon layer 14. In this embodiment, semiconductor substrate 10 is formed from silicon; however, semiconductor substrate 10 can be formed from different semiconductor materials in other embodiments (*e.g.*, Gallium Arsenide). Further, in this embodiment, insulating layer 12 is formed from a silicon oxide (*e.g.*, SiO_2), although in other embodiments insulating layer 12 can be formed from other non-conductive materials.

[0014] In one embodiment, semiconductor substrate 10, insulator layer 12 and silicon layer 14 are formed using known silicon on insulator (SOI) wafer fabrication processes. For example, the buried oxide layer (*i.e.*, insulating layer 12) can be formed using known oxygen implantation processes. Insulating layer 12, in this embodiment, has a thickness of about 1 μm, but can range from about 0.35 μm to 2 μm in other embodiments. Further, in this embodiment, silicon layer 14 is about 2.5 μm, but can range from about 1 μm to 10 μm in other embodiments.

[0015] Protective layer 16 is formed on silicon layer 14. In this embodiment, protective layer 16 is a silicon oxide formed using a suitable known process. For example, protective layer 16 can be formed by thermal oxidation of silicon layer 14, or using a low temperature oxide (LTO) deposition process. In one embodiment, protective layer 16 is formed from oxide with a thickness of about 5 μm. In other embodiments, the protective layer can have a different thickness. A thickness greater than 1 μm helps prevent lateral growth of an epitaxial silicon layer formed in a subsequent stage (described below) in fabricating the taper.

[0016] Although an oxide protective layer is described above, in other embodiments, protective layer 16 can be formed from other materials (*e.g.*, a silicon nitride material). Figure 1A illustrates a top view of the resulting structure (not to scale), with protective layer 16 being the only layer that is visible. However, the area occupied by the rib waveguide (*i.e.*, silicon layer 14) under protective layer 16 is indicated with dashed lines in Figure 1A.

[0017] Figure 2 illustrates a partial cross-section of the semiconductor workpiece (not to scale) during another stage in fabricating a taper, according to one embodiment of the present invention. In this stage, a photoresist layer 21 is formed on protective layer 16 and is patterned to define the taper using known photolithographic processes. In this embodiment, photoresist layer 21 is patterned so that it forms the inverse of the taper.

[0018] Figure 2A illustrates a top view of the resulting structure (not to scale). As shown, photoresist layer 21 is patterned so that a portion of protective layer 16 is

left uncovered. As will be described below, this uncovered portion defines the "foot print" of the taper to be formed in a subsequent stage of the taper fabrication process. In this embodiment, the wide end of the taper footprint has the same width as the waveguide formed by silicon layer 14, although in other embodiments, the width may be different. Further, the shape of the taper's footprint may be different in other embodiments (*e.g.*, triangular rather than pentagonal as in Figure 2A). The termination end of the taper footprint forms a relatively sharp angle (*e.g.*, a few degrees), although the termination end may be truncated in other embodiments.

[0019] Figure 3 illustrates a partial cross-section of the semiconductor workpiece (not to scale) during another stage in fabricating a taper, according to one embodiment of the present invention. In this stage, the uncovered portion of protective layer 16 (Figure 2) is etched so that silicon layer 14 is exposed, with the portion of protective layer 16 (Figure 2) under photoresist layer 21 (Figure 2) remaining intact. As shown in Figure 3, the remaining portion of the protective layer is indicated as protective layer 16A.

[0020] In one embodiment, a suitable known anisotropic etching process (*e.g.*, a dry etching process such as reactive ion etching) is used to etch the portion of protective layer 16 (Figure 2) left uncovered by photoresist layer 21 (Figure 2). In other embodiments, different etching processes can be used. Photoresist layer 21 (Figure 2) is then stripped or removed using standard photolithographic processes. A partial cross section of the resulting structure is represented in Figure 3. As shown in Figure 3, the termination end of the taper mask formed by protective

layer 16A is a point. In other embodiments, the termination need not be a point (*e.g.*, the termination end may appear as in Figure 3 but with the point truncated).

[0021] Figure 3A illustrates a top view of the resulting structure (not to scale). As shown, protective layer 16A is exposed after photoresist layer 21 (Figure 2) is removed. In addition, a portion of silicon layer 14 is exposed after the protective layer is etched.

[0022] Figure 4 illustrates a partial cross-section of the semiconductor workpiece (not to scale) during another stage in fabricating a taper, according to one embodiment of the present invention. In this stage, a silicon layer 41 is formed on the exposed portion of silicon layer 14. In one embodiment, a suitable known selective silicon epitaxy process in which silicon is "grown" on the exposed portion of silicon layer 14 while not growing on protective layer 16A. In one embodiment, silicon layer 41 has a thickness of about 4 μm; however, in other embodiments silicon layer 41 can have a thickness of about 2 μm to about 8 μm. The optimal thickness of silicon layer 41 can depend at least in part on the width or diameter of the larger waveguide (*e.g.*, optical fiber) to be coupled to the taper. The growth of silicon layer 41 is constrained by the side walls of protective layer 16A so that silicon layer 41 is formed in the desired taper shape. In one embodiment, the selective silicon epitaxy process is terminated when the thickness of silicon layer 41 reaches the thickness of protective layer 16A. In other embodiments, the growth of silicon layer 41 can be terminated before its thickness reaches that of protective layer 16A.

[0023] This stage of the taper fabrication process represents a significant improvement over conventional processes that etch silicon to form the taper. For example, as previously described, etching the silicon undesirably results in erosion or "erosion-like" effects at the narrow or point end of the taper, increasing loss. In addition, the upper surface of the silicon waveguide may be undesirably "roughened" by the etching process (*e.g.*, feature sensitivity), further increasing loss.

[0024] In contrast, by depositing silicon to form the taper in accordance with embodiments of the present invention, the point or narrow end of the taper is not eroded. Rather, the narrow end is essentially smooth and sharp, which tends to enhance performance of the resulting taper. In addition, the waveguide is not etched after protective layer 16 (Figure 2) is formed. Thus, the resulting upper surface of the waveguide (*i.e.* silicon layer 14) is significantly smoother than an etched surface. Consequently, the waveguide formed by silicon layer 14 will generally have less loss than one that is etched to form the taper.

[0025] In addition, selective silicon epitaxy processes can be sensitive to the surface topology of the growing surface (*e.g.*, micro-loading). In one embodiment, this topology sensitivity is taken advantage of to form silicon layer 41 with a sloped upper surface. That is, the selective silicon epitaxy process will tend to grow silicon at a slower rate near the narrow end of the taper because at that end, the sidewalls of protective layer 16A start getting closer and closer until they meet, changing the micro-loading in that area. As a result, the upper surface of silicon layer 41 will tend to slop downwards from the wide end of the taper to the narrow end of the taper as

indicated by surface 41A in Figure 4. This vertical slope of the taper can further increase the performance efficiency of the taper.

[0026] In other embodiments, a polysilicon layer can be deposited on protective layer 16A and then planarized by chemical mechanical polishing (CMP) so that the upper surface of protective layer 16A is exposed. However, this alternative embodiment can in some instances form the taper without the sloped upper surface that can be achieved using a selective silicon epitaxy process.

[0027] Figure 4A illustrates a top view of the resulting structure (not to scale). As shown, silicon layer 41 is visible, laterally surrounded by protective layer16A. In this embodiment, the termination end of the taper includes two surfaces that are angled so that the termination end is shaped like a wedge. As previously described, these surfaces of the wedge are not etched, which can advantageously increase the performance efficiency of the taper compared to conventional tapers that form the termination using etching processes.

[0028] Figure 5 illustrates a perspective view of a section cut as indicated in Figure 4, with protective layer 16A omitted so that the taper (*i.e.*, silicon layer 41) and the waveguide (*i.e.*, silicon layer 14) can be more easily appreciated. In addition to protective layer 16A, another protective layer (not shown) may be formed on silicon layer 41. As shown in Figure 5, the termination end (*i.e.*, end 51) of the taper includes surfaces that are angled with respect to the longitudinal axis of the taper. In this embodiment, the longitudinal axis is along the line connecting the center of the termination end 51 of the taper to the center of the wide end 52 of the taper.

[0029] Figure 6 illustrates a system 60 in which a waveguide taper according to embodiments of the present invention can be used. System 60 includes an optical signal source 61 connected to one end of an optical fiber 62. The other end of optical fiber 62 is connected to a PLC 63 that includes a taper 64. Taper 64 is fabricated according to one of the embodiments described above. For example, when the taper is implemented as shown in the embodiment of Figure 5, wide end 51 would be used to connect PLC 63 to the end of optical fiber 62. In one embodiment, PLC 63 is implemented in an integrated circuit. Other embodiments may have one or more other tapers (not shown) that are essentially identical in structure to taper 64.

[0030] Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable optical manner in one or more embodiments.

[0031] In addition, embodiments of the present description may be implemented not only within a semiconductor chip but also within machine-readable media or other electronic form. For example, the designs described above may be stored upon and/or embedded within machine readable media associated with a

design tool used for designing semiconductor devices. Examples include a netlist formatted in the VHSIC Hardware Description Language (VHDL) language, Verilog language or SPICE language. Some netlist examples include: a behavioral level netlist, a register transfer level (RTL) netlist, a gate level netlist and a transistor level netlist. Machine-readable media also include media having layout information such as a GDS-II file. Furthermore, netlist files or other machine-readable media for semiconductor chip design may be used in a simulation environment to perform the methods of the teachings described above.

[0032] Thus, embodiments of this invention may be used as or to support a software program executed upon some form of processing core (such as the CPU of a computer) or otherwise implemented or realized upon or within a machine-readable medium. A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (*e.g.*, a computer). For example, a machine-readable medium can include such as a read only memory (ROM); a random access memory (RAM); a magnetic disk storage media; an optical storage media; and a flash memory device, *etc.* In addition, a machine-readable medium can include propagated signals such as electrical, optical, acoustical or other form of propagated signals (*e.g.*, carrier waves, infrared signals, digital signals, *etc.*).

[0033] In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from

the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.